UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,920	02/02/2001	James J. Alwan	100.718.419 (MIC- 77US)	8909

7590 11/19/2004

RAJESH VALLABH, ESQ.
HALE & DORR, LLP
60 STATE STREET
BOSTON, MA 02109

EXAMINER	
MACCHIAROLO, PETER J	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,920	ALWAN, JAMES J.	
	Examiner	Art Unit	
	Peter J Macchiarolo	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The reply filed on 09/08/2004 consists of remarks related to the prior rejection of claims in the First Office Action. However, claims 13-26 are not allowable as explained below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of previously cited Sandhu et al (USPN 5271798; "Sandhu") in further view of previously cited Potter (USPN 5700176; "Potter").

3. In regards to claims 13-21, and 24, Applicant admits the prior art includes a method of forming an FED comprising providing a substrate having a central area and a peripheral area, forming alignment marks on the peripheral area of the substrate, forming an emitter electrode structure on the central area of the substrate, forming a plurality of micropoints in groups on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and plurality of micropoints, and depositing a conductive layer over the insulating layer in figure 1. Applicant further admits it is known that selectively etching openings through the conductive and insulating layers comprises applying a layer of photoresist on said conductive layer, imaging said photoresist to define a pattern for said openings, developing the photoresist,

and etching the pattern for the openings. The Examiner further notes this is a well known method of manufacture. Applicant further admits a method of making a semiconductor wafer to clear alignment marks by locally applying a wet etchant to uncover a structure is known in the art to effectively clear the marks without the use of photolithography[1] (see also Sandhu).

4. Neither Sandhu nor Applicant discloses that the recited method for clearing semiconductor wafer alignment marks can be used for FED fabrication.

5. However, Potter teaches a method of manufacturing a field emission device with fabrication processes and equipment similar to those used for semiconductor fabrication.[2] Further, Potter shows in figure 1, a cathode (100) and an anode (70) assembly assembled together in a FED, which can be automatically aligned, or aligned according to the well-known prior art method i.e. with alignment marks. Potter further teaches contact pads are selectively provided at the device top surface to make electrical contact, which will require the clearing method similar to Sandhu.

6. Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct an FED with the method admitted by Applicant and Sandhu to allow for a less costly manufacturing method.

7. In regards to claims 22, 23, 25 and 26, Applicant admits the prior art includes a method of forming a cathode assembly of a field emission device comprising providing a substrate, making alignment marks in a peripheral region of the substrate, forming an emitter electrode structure on a central region of the substrate, said central region being substantially surrounded

---

[1] Instant spec., page 4, para. 2.

by the peripheral region, forming a plurality of micropoints on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and plurality of micropoints, depositing a first conductive layer over the insulating layer, polishing the conductive layer via chemical-mechanical planarization, and etching openings through the conductive and insulating layers to expose the micropoints, with walls defining the openings being spaced away from the micropoints. The Examiner further notes this is a well-known method of manufacturing in the art of FED's.

8. Applicant further admits a method of making a semiconductor wafer to clear alignment marks by locally applying a wet etchant to uncover a structure is known in the art to effectively clear the marks without the use of photolithography[3] (see also Sandhu).

9. Neither Sandhu nor Applicant discloses that the semiconductor manufacturing method comprising selectively spraying a wet etchant on a structure can be used for FED fabrication.

10. However, in view of Potter's teaching and the above discussion and, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct an FED with the method admitted by Applicant and Sandhu to allow for less pure materials and cheaper manufacturing method.

Response to Arguments

11. Applicant's arguments filed 09/08/2004 have been fully considered but are not persuasive.

---

[2] Potter, abstract, and col. 23-29.
[3] Instant spec., page 4, para. 2.

12. Firstly, Applicant alleges that the background of the Application does not provide any disclosure or suggestion for selectively etching through the conductive and insulating layers, as defined in the instant claims. However, the Examiner respectfully asserts that Applicant has misread the previous rejection. The citation in question reads, "Instant spec., page 4, para. 2," (emphasis added) or the paragraph which begins, "Micron Technology, Inc. has developed certain equipment used specifically in the field of semiconductor wafer fabrication for the purpose of clearing alignment marks. The equipment includes nozzles that selectively spray a wet etchant over the alignment marks while limiting application of the etchant over other parts of the wafer," (emphasis added). This passage, along with Sandhu, are relied upon in the previous rejection to show that the method of manufacturing a semiconductor wafer using selective wet etchant to uncover alignment marks is known.[4] Merely applying this known manufacturing method (the selective wet etchant method) to a known device (the conventional FED as discussed at page 2, numbered paragraph 3 of the previous office action) is not novel.

13. Furthermore, neither said passage nor Sandhu discloses that photolithography is needed to aid in the removal of the alignment marks, therefore, the disclosed methods are known in the art to remove the alignment marks without using photolithography.

14. Secondly, Applicant alleges Potter does not disclose or suggest the issue of selective etching as set forth in Applicant's claimed invention. The Examiner respectively asserts that this argument is not relevant, since Potter was relied upon, as discussed in the previous Office Action at page 3, numbered paragraph 6, as evidence that using a semiconductor wafer manufacturing method can be applied to an FED with a realistic expectation of success. In the abstract and

[4] Previous rejection, page 3, numbered paragraph 4.

column 1, lines 29-30, Potter recites, "A fabrication process is disclosed using process steps (S1-S18) similar to those of semiconductor integrated circuit fabrication to produce the novel devices [FED's] and their arrays," (emphasis added).

15. Thirdly, Applicant alleges that the previous Office Action has failed to make a *prima facie* case of obviousness. The Examiner respectfully disagrees and lists the three basic criteria which can be found in the previous Office Action.

a. Both Applicant's admitted prior art and Sandhu disclose that using the manufacturing method of selectively spraying a wet etchant onto a semiconductor wafer for the purpose of clearing alignment marks eliminates the use of expensive photolithography. This suggests that manufacturing methods requiring photolithography to clear alignment marks may become less expensive by selectively spraying a wet etchant onto the alignment marks instead of using photolithography.

b. Potter is evidence that there is a realistic expectation of success (see numbered paragraph 15 above).

c. Finally, not only is the claimed general method of manufacturing an FED well known, but Applicant's admitted prior art also discloses and suggests the claimed FED structure, general method of manufacturing the FED, and etching openings to expose the micropoints at figure 1, while Sandhu teaches selectively applying a wet etchant on alignment marks (see previous Office Action).

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter J Macchiarolo whose telephone number is (571) 272-2375. The examiner can normally be reached on 8:30 - 5:00, M-F.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571) 272-2475. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pm

Joseph Williams
Primary Examiner
AU 2879